

WHAT IS CLAIMED IS:

- 1 1. A method of fabricating a semiconductor device, comprising:
 - 2 providing an intermediate structure having a top surface, wherein an isolation trench is
 - 3 formed in the intermediate structure;
 - 4 depositing isolation material over the intermediate structure, wherein the isolation
 - 5 material fills the isolation trench and wherein excess isolation material extends above the top
 - 6 surface of the intermediate structure;
 - 7 removing part of the excess isolation material until there is a predetermined thickness of
 - 8 isolation material remaining on the top surface of the intermediate structure;
 - 9 forming a contact opening in the isolation material at the isolation trench, wherein the
 - 10 contact opening extends through at least part of the intermediate structure;
 - 11 depositing contact material over the isolation material, wherein the contact material fills
 - 12 the contact opening;
 - 13 removing excess contact material, if any, that extends above the isolation material; and
 - 14 removing the excess isolation material at least until the top surface of the intermediate
 - 15 structure is reached.
- 1 2. The method of claim 1, wherein the semiconductor device includes transistors.
- 1 3. The method of claim 1, wherein the isolation material is selected from a group consisting
2 of undoped silicon glass, HDP oxide, undoped polysilicon, oxide, spun-on dielectric material,
3 and flow oxide.

1 4. The method of claim 1, wherein the contact material comprises a material selected from a
2 group consisting of polysilicon, metal, tungsten, aluminum, aluminum copper, copper, and
3 combinations thereof.

1 5. The method of claim 1, wherein the predetermined thickness is between about 500 and
2 about 1000 Å.

1 6. The method of claim 1, wherein the removing part of the excess isolation material is
2 performed using chemical mechanical polishing.

1 7. The method of claim 1, wherein the removing excess contact material is performed using
2 chemical mechanical polishing.

1 8. The method of claim 7, wherein the removing the excess isolation material until the top
2 surface of the intermediate structure is reached, is performed by continuing the same chemical
3 mechanical polishing process used to remove excess contact material.

1 9. The method of claim 1, wherein the removing the excess isolation material until the top
2 surface of the intermediate structure is reached, is performed using chemical mechanical
3 polishing.

1 10. The method of claim 1, wherein the intermediate structure comprises a substrate, a
2 bottom insulator layer, a semiconducting material layer, and a pad nitride layer, the bottom
3 insulator layer being formed over the substrate, the semiconducting material layer being formed
4 over the bottom insulator layer, and the pad nitride layer being formed over the semiconducting
5 material layer.

- 1 11. The method of claim 10, wherein the substrate comprises silicon.
- 1 12. The method of claim 10, wherein the bottom insulator layer is selected from a group
2 consisting of undoped oxide, silicon dioxide, and silicon nitride.
- 1 13. The method of claim 10, wherein the semiconducting material layer is selected from a
2 group consisting of silicon, silicon germanium, germanium, and GaAs.
- 1 14. The method of claim 10, wherein the intermediate structure further comprises a pad oxide
2 layer located between the semiconducting material layer and the pad nitride layer.

1 15. A method of fabricating a semiconductor device, comprising:
2 providing an intermediate structure comprising a substrate, a bottom insulator layer, a
3 semiconducting material layer, and a pad nitride layer, wherein the bottom insulator layer is
4 formed over the substrate, the semiconducting material layer is formed over the bottom insulator
5 layer, and the pad nitride layer is formed over the semiconducting material layer;
6 forming an isolation trench in the pad nitride layer and the semiconducting material layer;
7 depositing an isolation material over the structure, wherein the trenches are filled with the
8 isolation material and excess isolation material extends above the pad nitride layer;
9 removing part of the excess isolation material such that a predetermined thickness of the
10 isolation material remains atop the pad nitride layer;
11 forming a contact opening in the isolation material within the isolation trench, extending
12 through the bottom insulator layer, and opening to the substrate;
13 depositing a contact material over the structure, wherein the contact material fills the
14 contact opening and excess contact material extends above a top surface of isolation material;
15 removing the excess contact material down to the top surface of the isolation material;
16 and
17 removing the excess isolation material at least until the pad nitride layer is reached.

1 16. The method of claim 15, further comprising:
2 doping the substrate at the contact opening to form a P+ implant region in the substrate.

1 17. The method of claim 16, wherein the doping is performed using a material selected from
2 a group consisting of B and BF₂.

1 18. The method of claim 15, wherein the contact material comprises a material selected from
2 a group consisting of polysilicon, metal, tungsten, aluminum, aluminum copper, copper, and
3 combinations thereof.

1 19. The method of claim 18, further comprising:
2 doping the contact material to make it conductive.

1 20. The method of claim 15, wherein the semiconductor device includes transistors.

1 21. The method of claim 15, wherein the isolation material is selected from a group
2 consisting of undoped silicon glass, HDP oxide, undoped polysilicon, oxide, spun-on dielectric
3 material, and flow oxide.

1 22. The method of claim 15, wherein the predetermined thickness is between about 500 and
2 about 1000 Å.

1 23. The method of claim 15, wherein the removing part of the excess isolation material is
2 performed using chemical mechanical polishing.

1 24. The method of claim 15, wherein the removing excess contact material is performed
2 using chemical mechanical polishing.

1 25. The method of claim 24, wherein the removing the excess isolation material until the pad
2 nitride layer is reached, is performed by continuing the same chemical mechanical polishing
3 process used to remove excess contact material.

- 1 26. The method of claim 15, wherein the intermediate structure further comprises a pad oxide
- 2 layer located between the semiconducting material layer and the pad nitride layer.

1 27. A semiconductor device, comprising:
2 isolation trenches formed in a structure, wherein the isolation trenches are filled with
3 isolation material; and
4 a contact formed through one of the isolation trenches and filled with contact material,
5 wherein no residual contact material from forming the contact remains atop another trench of the
6 isolation trenches.